

82878

J1036 U.S. PTO
09/940010



714	724	Subclass
Class	ISSUE CLASSIFICATION	

PATENT NUMBER

6546512



6546512

U.S. UTILITY Patent Application

O.I.P.E. SCANNED <i>KC</i> <i>CTH</i> <i>Am</i> O.A.	PATENT DATE APR 08 2003
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APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/940010	D	714	724	2133 2133	Chase

APPLICANTS
Roland Ochoa
Gregory Cowan
Kim Pierce

TITLE
Semiconductor integrated circuit having compression circuitry for compressing test data, and the test system and method for utilizing the semiconductor integrated circuit

PTO-2040
12/99

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ISSUING CLASSIFICATION							
ORIGINAL		CROSS REFERENCE(S)					
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
714	724	324	765				
INTERNATIONAL CLASSIFICATION							
G 01 R 31/28							

☐ Continued on Issue Slip Inside File Jacket

1-1503 Formal Drawings 5 sheets 8-27-01

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. 5	Figs. Drwg. 5	Print Fig. 2	Total Claims 14	Print Claim for O.G. 7
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	Shelly A Chase 9-5-02 (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED 9-10-02	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____	ALBERT DECADY SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2100 A Decady 9/9/02 (Primary Examiner) (Date)			ISSUE FEE <i>W</i> Amount Due \$1280.00 Date Paid 12-3-02	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	V. J. 9-15-02 (Legal Instruments Examiner) (Date)			ISSUE BATCH NUMBER	

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Formal Drawings 5 sheets 351

Issue Fee

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